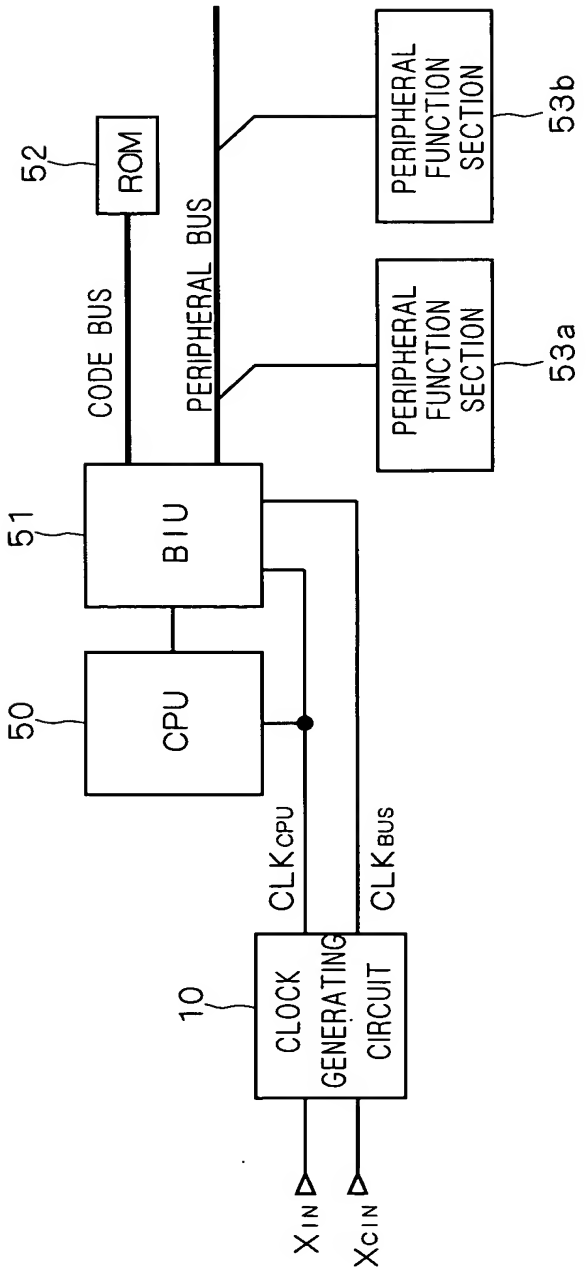

52
ROM
CODE BUS
PERIPHERAL BUS
PERIPHERAL FUNCTION SECTION
53b
PERIPHERAL FUNCTION SECTION
53a
51
BIU
50
CPU
CLKCPU
CLKBUS
10
CLOCK GENERATING CIRCUIT
XIN
XCIN

FIG. 1

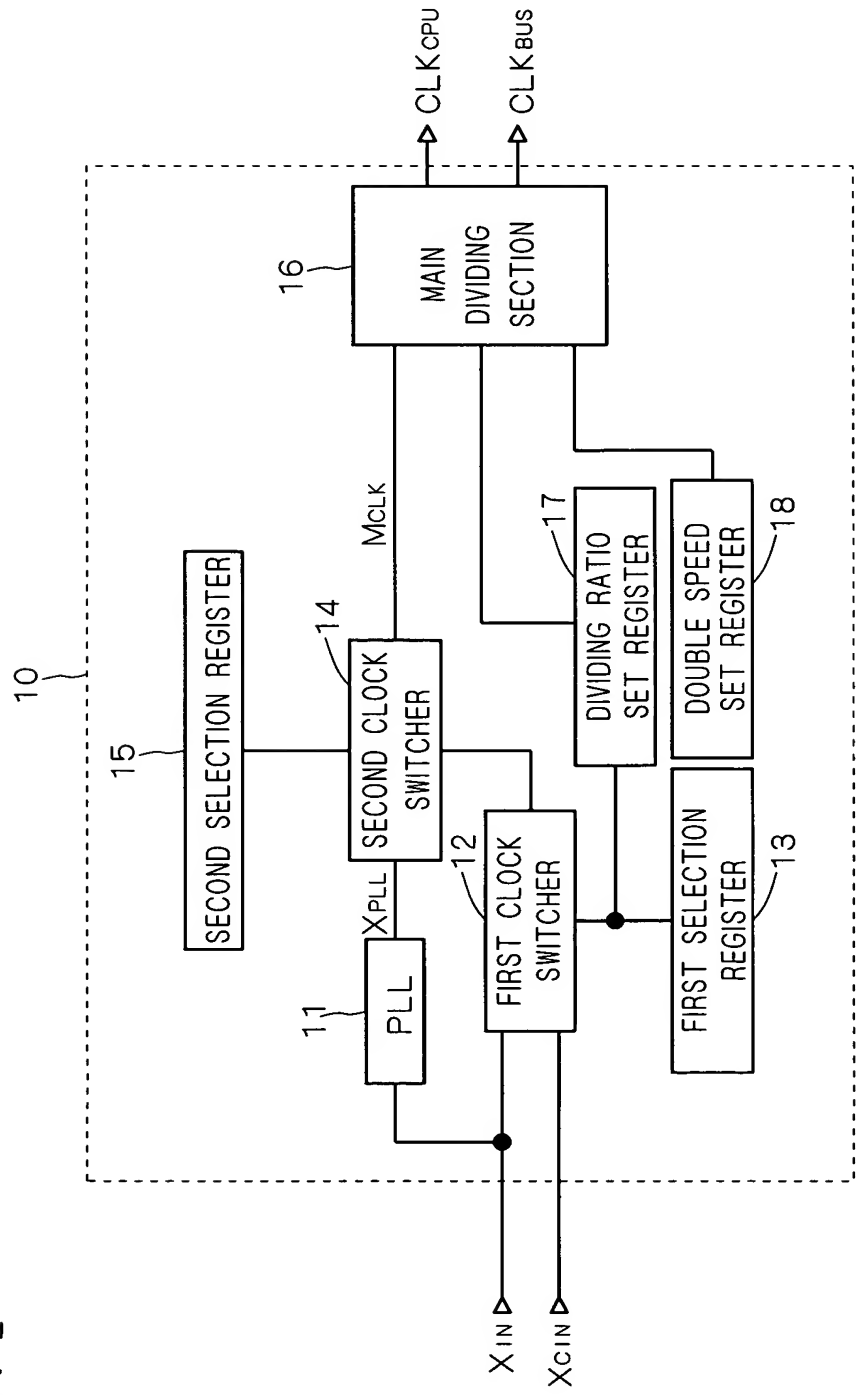

CLKCPU
CLKBUS
16
MAIN DIVIDING SECTION
MCLK
17
DIVIDING RATIO SET REGISTER
18
DOUBLE SPEED SET REGISTER
10
15
SECOND SELECTION REGISTER
14
SECOND CLOCK SWITCHER
XPLL
12
FIRST CLOCK SWITCHER
FIRST SELECTION REGISTER
13
11
PLL
XIN
XCIN

FIG. 2

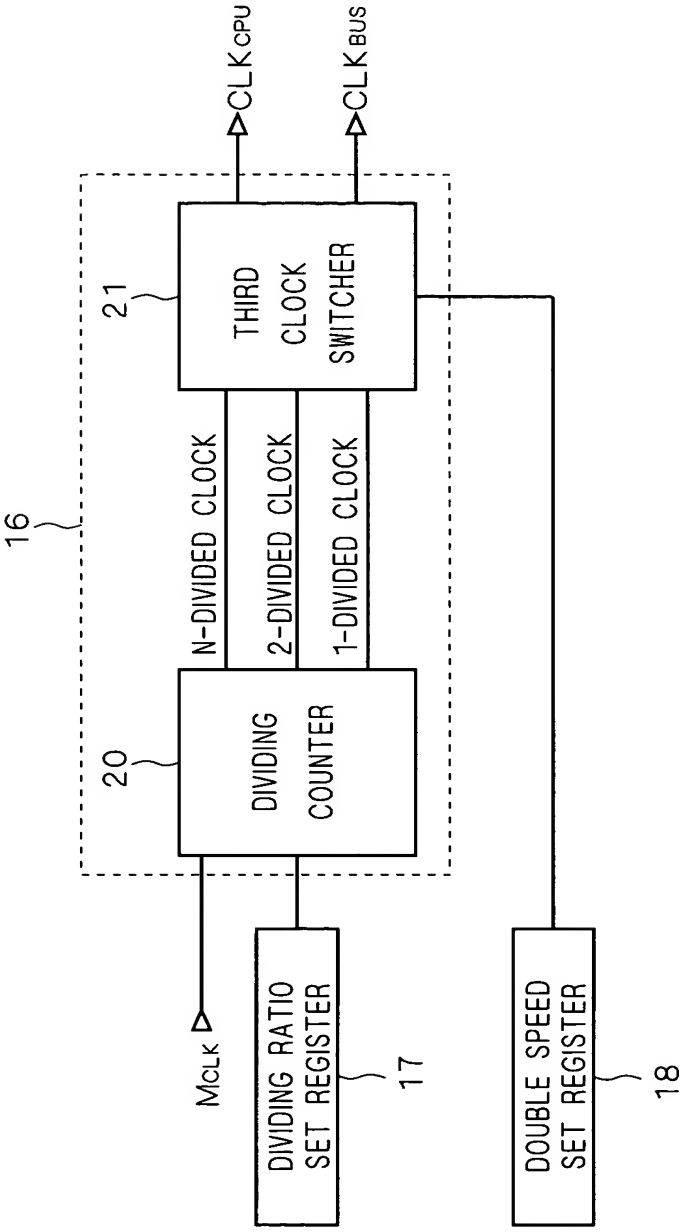

CLK CPU
CLK BUS
21
THIRD CLOCK SWITCHER
16
N-DIVIDED CLOCK
2-DIVIDED CLOCK
1-DIVIDED CLOCK
20
DIVIDING COUNTER
MCLK
DIVIDING RATIO SET REGISTER
17
DOUBLE SPEED SET REGISTER
18

FIG. 3

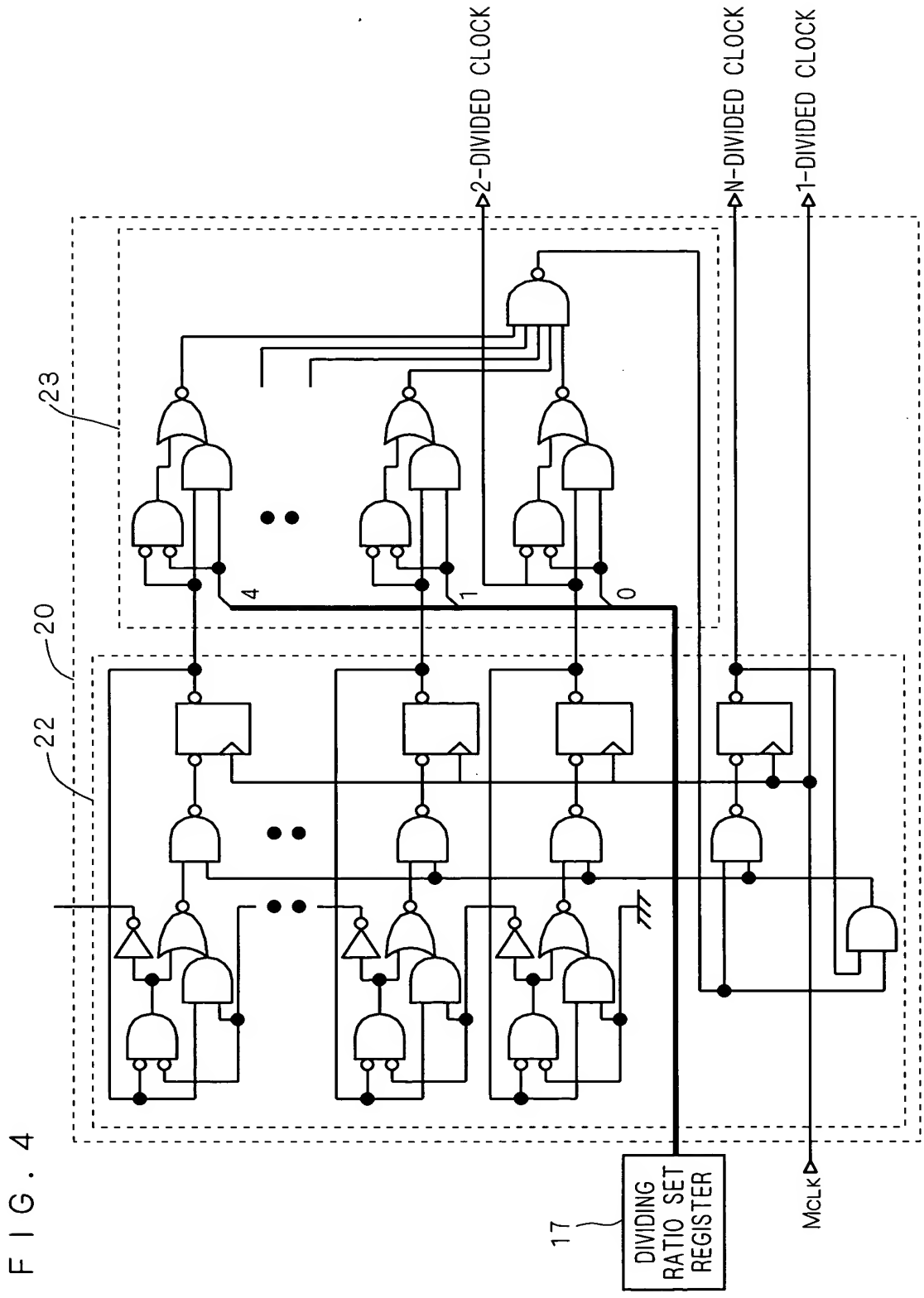

2-DIVIDED CLOCK
N-DIVIDED CLOCK
1-DIVIDED CLOCK
23
20
22
4
1
0
17
DIVIDING RATIO SET REGISTER
MCLK

FIG. 4

FIG. 5

	OUTPUT OF THIRD CLOCK SELECTOR 21		SETTING OF DOUBLE SPEED SET REGISTER 18		
OPERATION MODE CLASSIFICATION	CLK_{CPU}	CLK_{BUS}	b 1	b 2	b 3
X_{IN} (X_{CIN})	1-DIVIDED CLOCK	1-DIVIDED CLOCK	0	0	1
$X_{IN}/2$ ($X_{CIN}/2$)	2-DIVIDED CLOCK	2-DIVIDED CLOCK	0	1	0
DOUBLE SPEED	2-DIVIDED CLOCK	N-DIVIDED CLOCK	1	0	0
N-DIVIDING	N-DIVIDED CLOCK	N-DIVIDED CLOCK	0	0	0

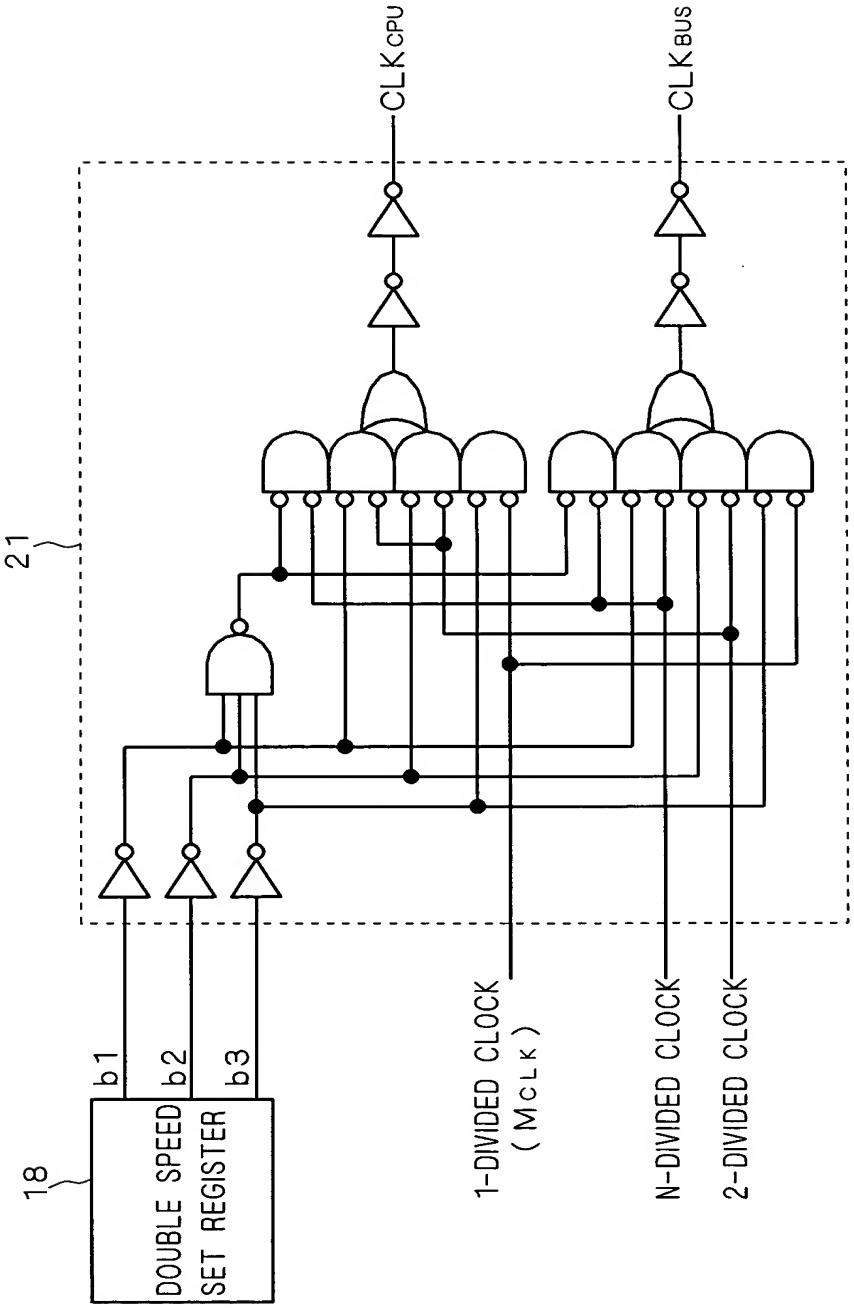
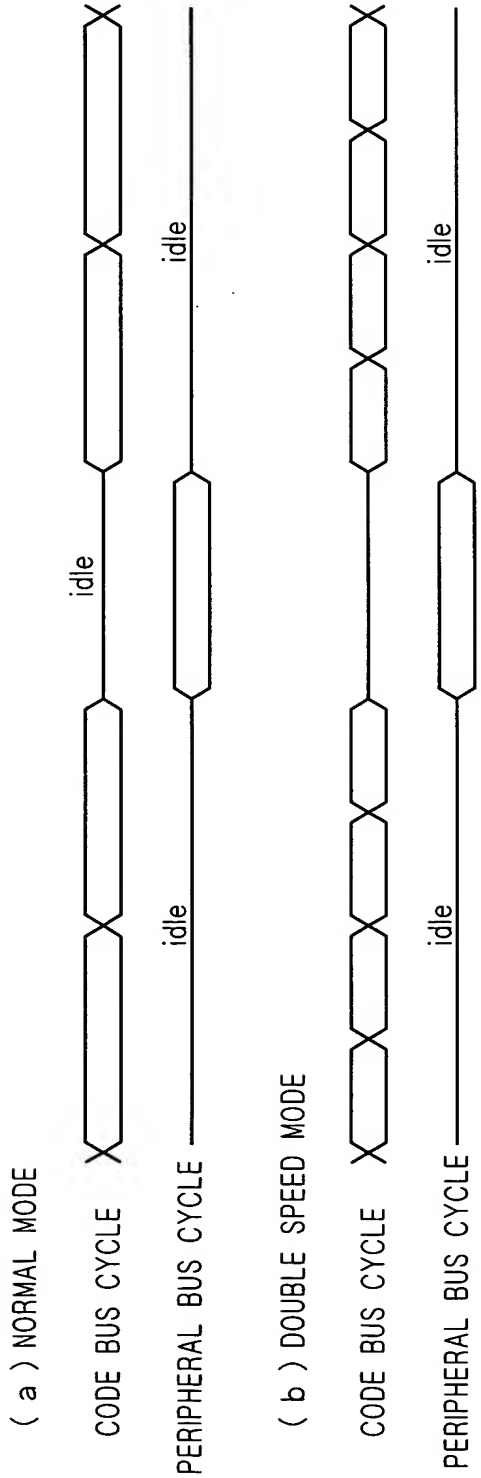

CLKCPU
CLKBUS
21
b1
b2
b3
18
DOUBLE SPEED SET REGISTER
1-DIVIDED CLOCK (MCLK)
N-DIVIDED CLOCK
2-DIVIDED CLOCK

FIG. 6

FIG. 7


(a) NORMAL MODE
CODE BUS CYCLE
idle
PERIPHERAL BUS CYCLE
idle
(b) DOUBLE SPEED MODE
CODE BUS CYCLE
PERIPHERAL BUS CYCLE
idle
idle

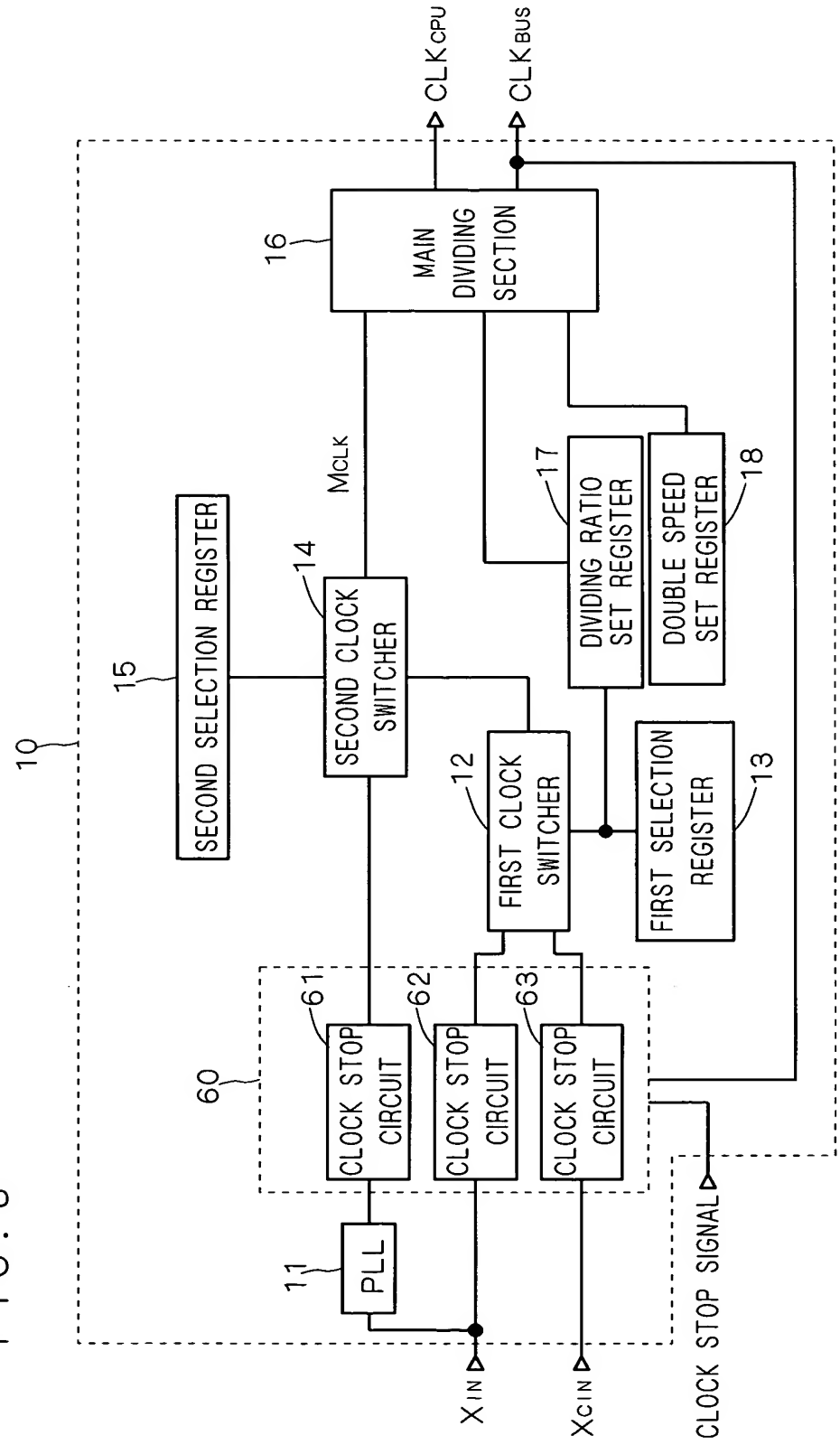
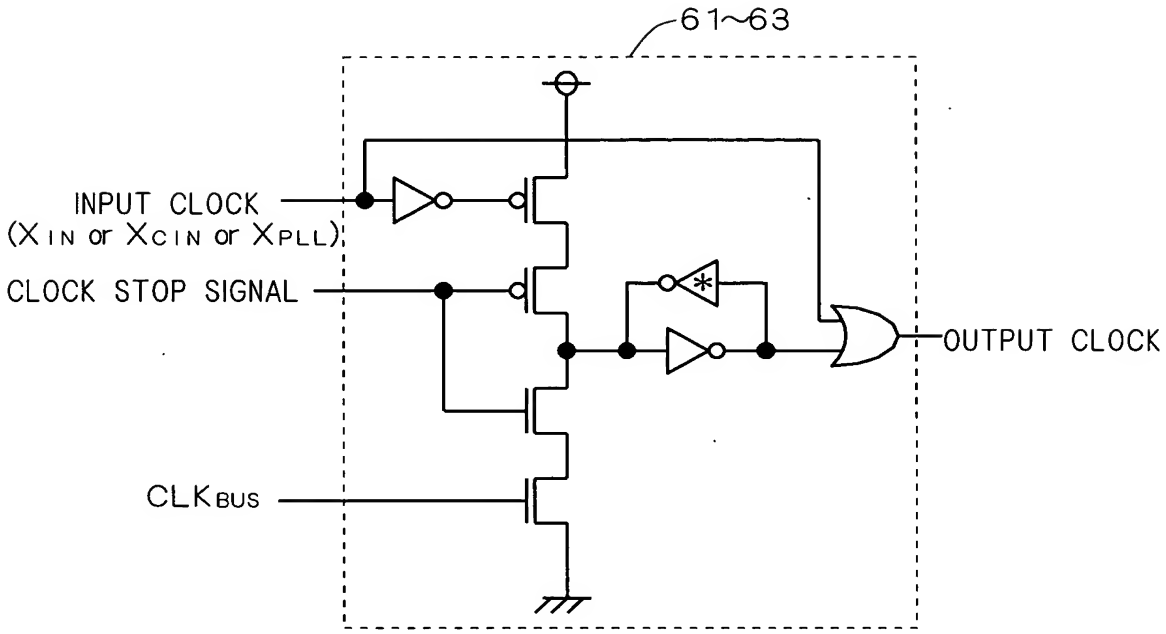

CLKCPU
CLKBUS
16
MAIN DIVIDING SECTION
MCLK
17
DIVIDING RATIO SET REGISTER
18
DOUBLE SPEED SET REGISTER
15
SECOND SELECTION REGISTER
14
SECOND CLOCK SWITCHER
10
12
FIRST CLOCK SWITCHER
13
FIRST SELECTION REGISTER
60
61
62
63
CLOCK STOP CIRCUIT
CLOCK STOP CIRCUIT
CLOCK STOP CIRCUIT
11
PLL
XIN
XCIN
CLOCK STOP SIGNAL

FIG. 8

FIG. 9


61~63
INPUT CLOCK
(XIN or XCIN or XPLL)
CLOCK STOP SIGNAL
CLKBUS
OUTPUT CLOCK

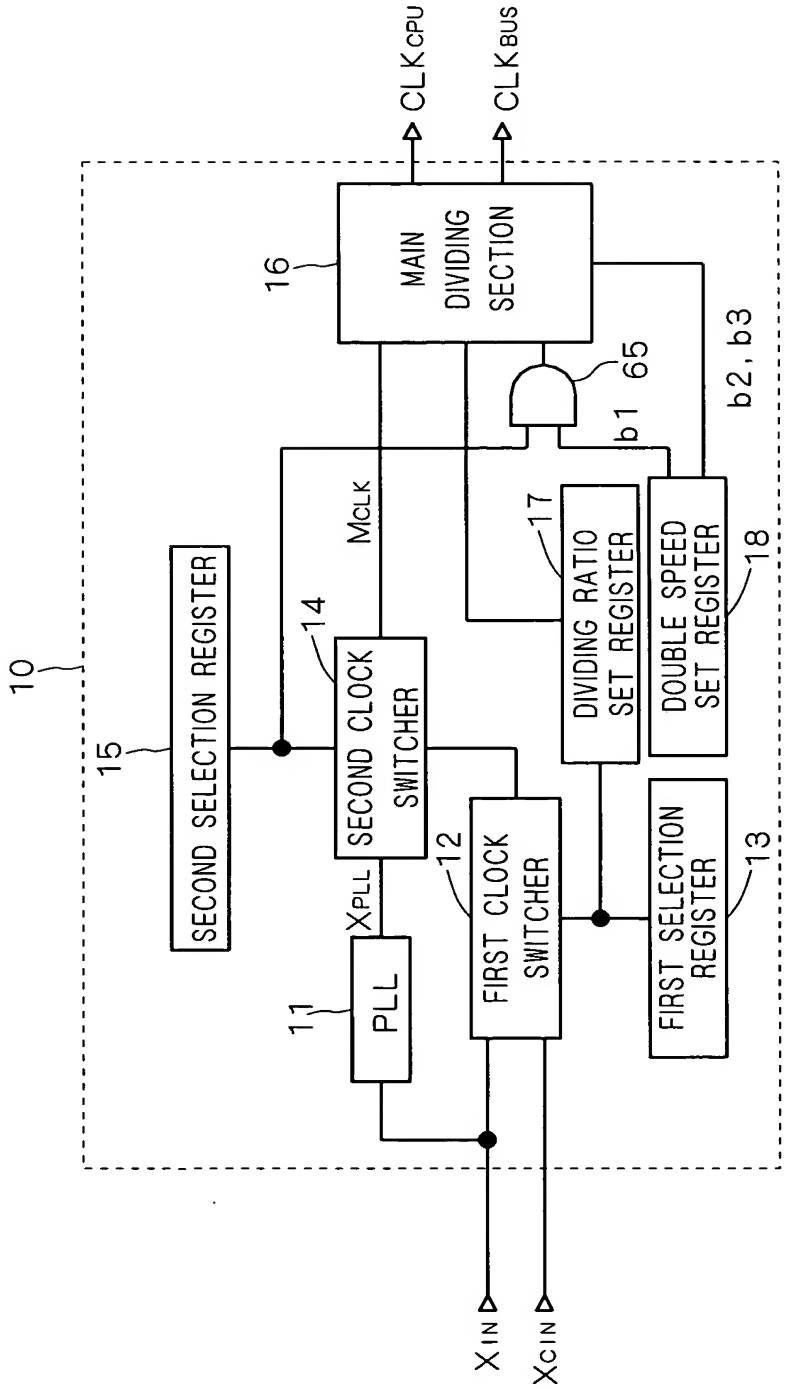

CLKCPU
CLKBUS
16
MAIN DIVIDING SECTION
65
b1
b2, b3
MCLK
17
DIVIDING RATIO SET REGISTER
DOUBLE SPEED SET REGISTER
18
10
15
SECOND SELECTION REGISTER
14
SECOND CLOCK SWITCHER
XPLL
12
FIRST CLOCK SWITCHER
FIRST SELECTION REGISTER
13
11
PLL
XIN
XCIN

FIG. 10

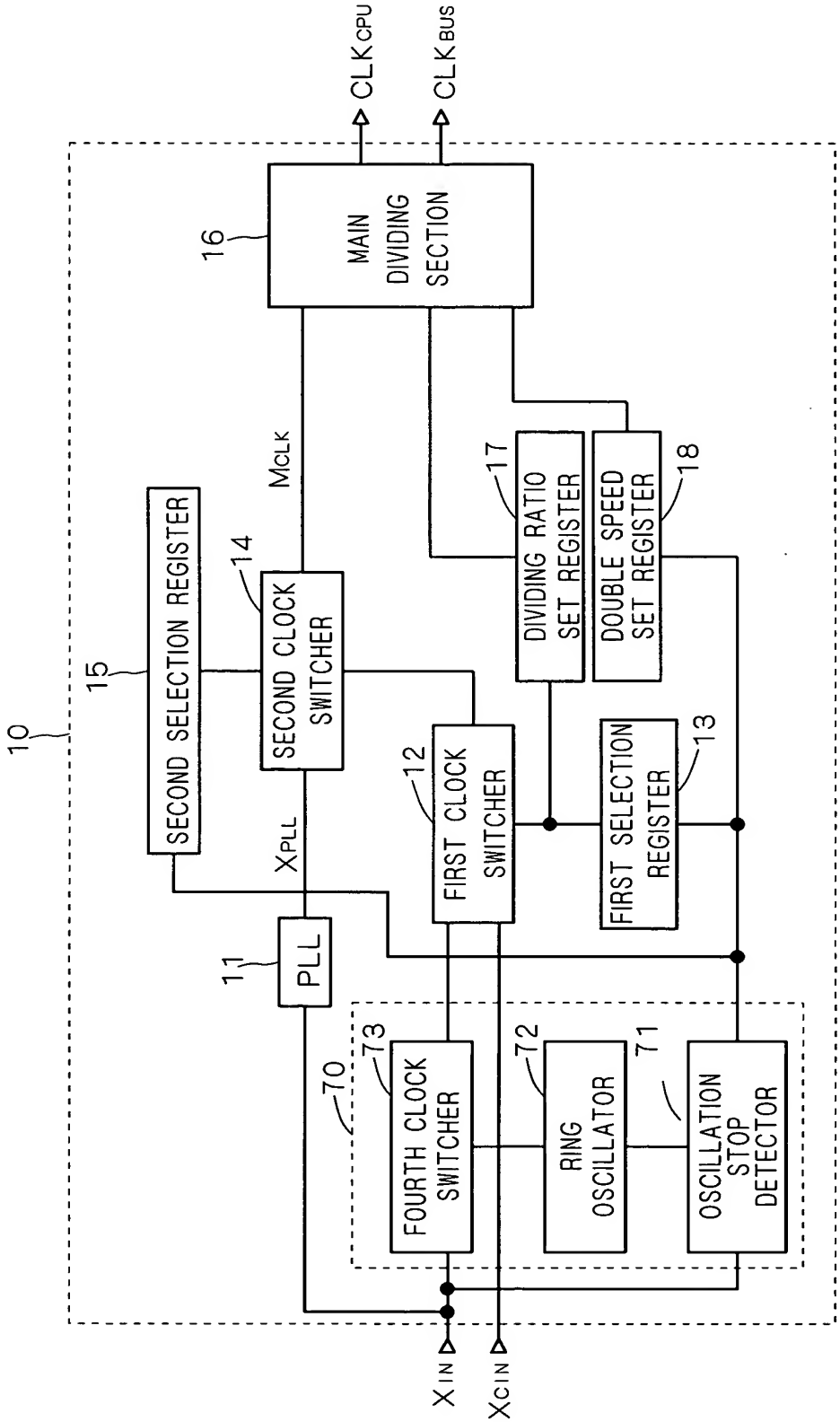

CLKCPU
CLKBUS
16
MAIN DIVIDING SECTION
MCLK
17
DIVIDING RATIO SET REGISTER
18
DOUBLE SPEED SET REGISTER
14
SECOND CLOCK SWITCHER
15
SECOND SELECTION REGISTER
10
12
FIRST CLOCK SWITCHER
13
FIRST SELECTION REGISTER
XPLL
11
PLL
70
73
FOURTH CLOCK SWITCHER
72
RING OSCILLATOR
71
OSCILLATION STOP DETECTOR
XIN
XCIN

FIG. 11